R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicants' representative thanks Examiner Gerstl for the indications of allowable matter in claims 4, 11, 17 and 18.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and the new claims may be found in the specification, for example, on page 7 lines 8-13, page 12 lines 3-16 and FIG. 5, as originally filed, and claims 2, 12 and 16, as previously presented. Thus, no new matter has been added.

CLAIM OBJECTIONS

The objections to claims 16-18 for informalities have been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 3, 5, 15 and 16 under 35 U.S.C. §102(b) as being anticipated by Mirapuri et al. '294 (hereafter Mirapuri) has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

Mirapuri concerns a method and apparatus for restarting pipeline processing (Title). In contrast, claim 1 provides (in part) a step for setting first status unique to a first operand data stored in a first register. In contrast, Mirapuri appears to be silent regarding status information unique to operand data. The control registers of Mirapuri relied upon in the rejection store "information which identifies whether **the corresponding pipeline stage** contains a valid instruction or an invalid instruction" (Mirapuri, column 9 lines 39-42, emphasis added). Therefore, Mirapuri does not appear to disclose or suggest a step for setting first status unique to a first operand data stored in a first register as presently claimed. Claim 15 provides language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides a step for setting a first status to an invalid state in response to a first register receiving a second operand data from a second register having a second status in the invalid state prior to transferring the second operand data to the first register. In contrast, Mirapuri appears to be silent regarding transferring operand data from one register to another where the starting operand data is know invalid. Therefore, Mirapuri does not appear to disclose or suggest a step for setting a first status to an invalid state in response to a first register receiving a second operand data from a second register having a

second status in the invalid state prior to transferring the second operand data to the first register as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 5 depends from allowable claim 4 and thus contains all of the limitation of claim 4. As such, claim 5 is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 8, 10, 12, 13, 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Steiss '420 has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

The rejection of claims 2 and 7 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Sites '167 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 9 and 14 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Sites and Steiss has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 6 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Blomgren '109 has been obviated by appropriate amendment and should be withdrawn.

Mirapuri concerns a method and apparatus for restarting pipeline processing (Title). Sites concerns ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system (Title). Steiss concerns a microprocessor arithmetic logic unit using multiple number representations (Title). Blomgren concerns an address tracking and branch resolution in a processor with multiple execution pipelines and instruction stream discontinuities (Title).

Claim 8 provides (in part) a first buffer configured to buffer a first status unique to a first operand data and logic configured to stall a processor in response to both (a) an instruction requiring the first operand data and (b) the first status being in an invalid state. In contrast, Mirapuri appears to be silent regarding status information unique to operand data. Furthermore, no motivation appears to exist to modify Mirapuri to stall a processor pipeline in response to a "V" bit taught by Steiss. In particular, Mirapuri already provides a mechanism for stalling a processor pipeline without using a new bit that indicates that data is not available. Therefore, no motivation appears to exist to combine or modify the references.

Furthermore, the assertion on page 11 of the Office Action that having status bits in the same register as the associated data bits would provide motivation "for the purpose of convenience in location and logical speedup" does not appear to be

taught by either Mirapuri, Steiss or knowledge generally available to one of ordinary skill in the art. No evidence or convincing line of reasoning has been presented in the Office Action that the circuitry receiving the data from a particular data register is conveniently located to the circuitry receiving the status, also stored in the particular data register. Furthermore, the argument that placing the data and status in the same particular data register would somehow result in a logical speedup is merely a conclusory statement lacking any supporting evidence. Therefore, *prima facie* obviousness to combine the references has not been established. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 10 provides logic configured to set a first status to an invalid state in response to receiving a second operand data from a second register having a second status in the invalid state prior to transferring the second operand data to the first register. In contrast, both Mirapuri and Steiss appear to be silent regarding transferring known invalid data from one register to another. Therefore, Mirapuri and Steiss, alone or in combination, do not appear to disclose or suggest logic configured to set a first status to an invalid state in response to receiving a second operand data from a second register having a second status in the invalid state prior to transferring the second operand data to the first register as presently claimed. As such, claim 10 is

fully patentable over the cited references and the rejection should be withdrawn.

Claim 12 depends from the allowable claim 11 and thus contains all of the limitations of claim 11. As such, claim 12 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 19 provides a first logic gate configured to combine a plurality of bits of a first status read from a first register. In contrast, both Mirapuri and Steiss appear to be silent regarding a logic gate for combining bits of a status read from a register. Furthermore, the cite to Blomgren in the rejection does not appear to be proper as Blomgren is not part of the basis for rejection. Therefore, Mirapuri and Steiss, alone or in combination, do not appear to teach or suggest a first logic gate configured to combine a plurality of bits of a first status read from a first register as presently claimed. As such, claim 19 is fully patentable over the cited references and the rejection should be withdrawn.

Regarding claim 6, *prima facie* obviousness has not been established for lack of clear and particular evidence of motivation to combine the references. In particular, the alleged motivation on page 20 of the Office Action "so that a low-cost address tracking scheme is realized" is not credited to either Mirapuri, BBB or knowledge generally available to one of ordinary skill in

the art. Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). No evidence or explanation has been provided why one of ordinary skill in the art would want to add a low-cost address tracking scheme to Mirapuri. Therefore, the alleged motivation appears to be merely a conclusory statement. As such, claim 6 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2, 7, 9, 13, 14 and 20 depended either from independent claims 1 or 8, which are now believed to be allowable. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

ALLOWABLE SUBJECT MATTER

Allowable claim 4 has been rewritten in independent form incorporating a portion of intervening claim 2 for antecedent basis purposes. Allowable claim 11 has been rewritten in independent form to include all limitations of the base claim (claim 11 had no intervening claims). Allowable claim 17 has been rewritten in independent form incorporating a portion of intervening claim 16 for antecedent basis purposes.

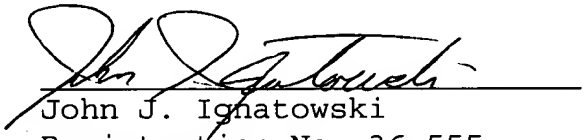
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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